

COMPASS

a FormFactor users' group conference



High Parallelism Testing of Advanced Image Sensors

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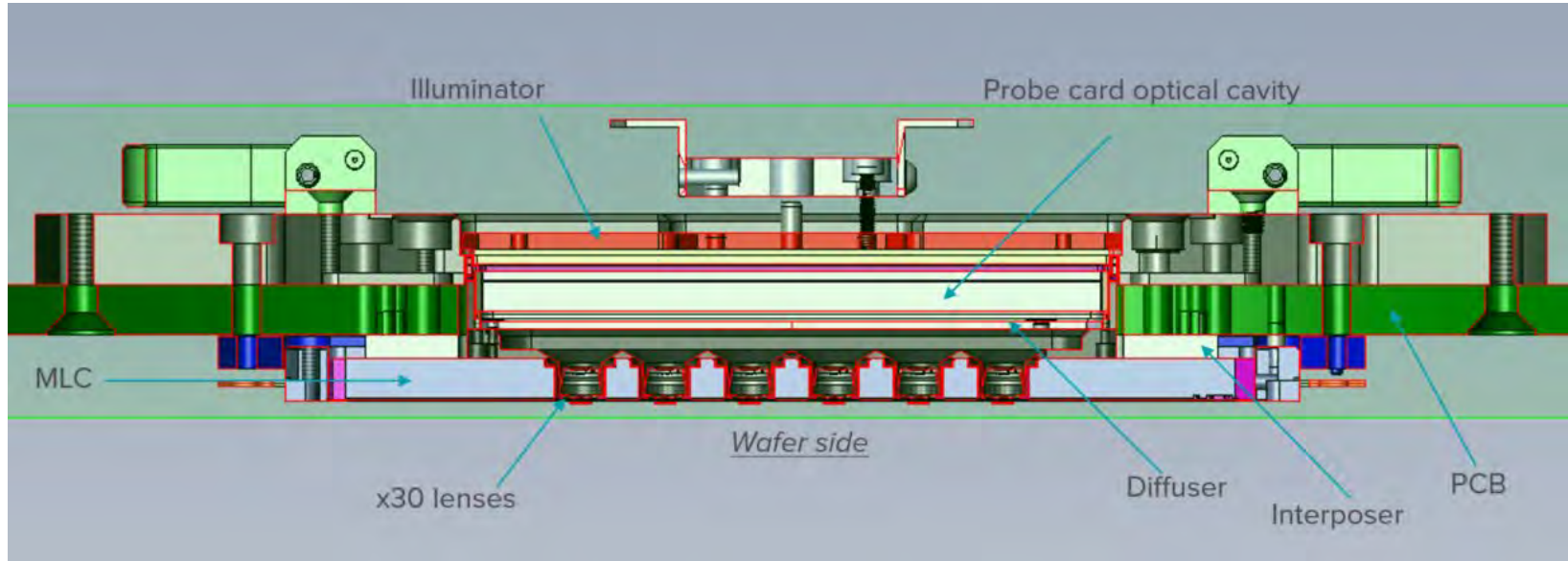


Technical challenges

- **Parallel by 30 sites test solution**
 - Complex optical stack integration embedding illuminator & lenses
 - Industrial environment, from -20°C to 90°C, must be robust and easy to set-up
- **Mechanical specification**
 - Lens placement tolerance must not exceed +/- 35 um for X and Y, +/- 25 um for Z
- **Optical performances**
 - Optical gain & light signal uniformity within device under test must be repeatable
 - Site-to-site but also probe card to probe card (> tens of PC)
 - Stable along probe card life time
- **Electrical**
 - High speed signal integrity such as CSI2 @1.5 Gbps

Probe card overview

- Illuminator & diffuser mounted on PC, probe head embedding x30 lens modules



(Fig. 1)

Optical stack



(Fig. 2)

L4: ILLUMINATOR (common to all site)

L3: Lambertian diffuser (common to all site)

L2: Optical MLC frame (x30 lens barrels)

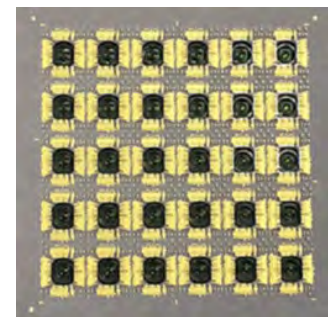
L1: Aspherical lens module (per site)

L0: Wafer/sensor level



(Fig. 3a)

Diffuser
side



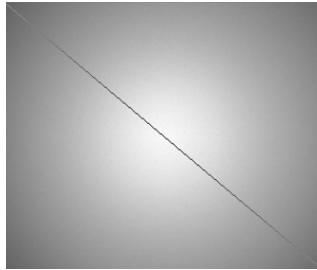
(Fig. 3b)

Sensor/tips
side

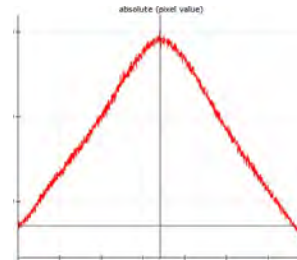
x30 probe head
Top & bottom view

Lens X/Y placement and vignetting

- Brightness is reduced in the sensor corners compared to the center due lens vignetting
- To ensure site-to-site light uniformity, proper lens X/Y positioning is critical
 - Maximum brightness to be in the center of the pixel array and at expectable level
- Light level must be well balanced between the 4 corners within DUT



(Fig. 4a)



(Fig. 4b)

Image signal profile from Top Left
Corner to Bottom Right corner

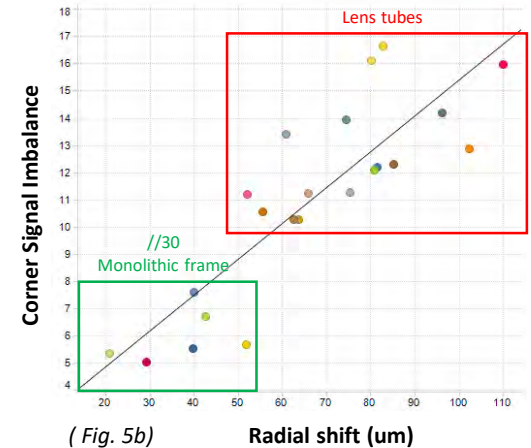
Lens X/Y centering and optical performance

- Lens X/Y placement ensured by monolithic mechanical frame
 - 1 lens holder for 30 sites pre-machined in spec
 - Better accuracy of lens positioning vs previous integration assembling lens tubes in MLC
 - Faster frame adjustment, only one X/Y offset overall tuning (no site-to-site)
- Good reproducibility from probe card to probe card



(Fig. 5a)

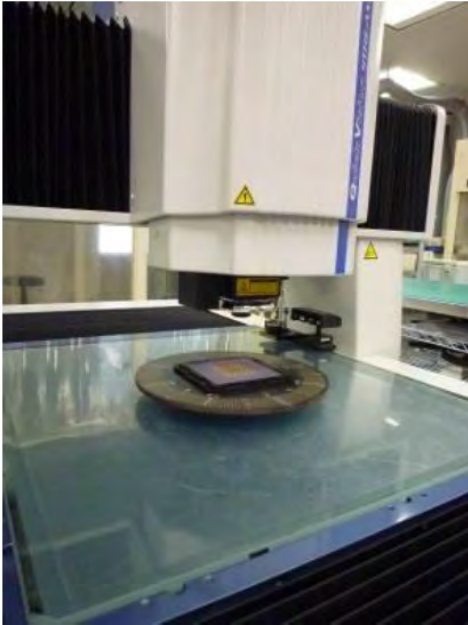
Ex. of light uniformity per site
using monolithic frame



(Fig. 5b)

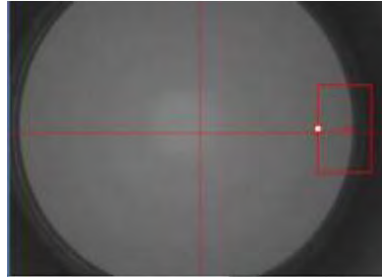
Lens frame alignment

- Lens alignment target $\pm 35 \mu\text{m}$ X/Y

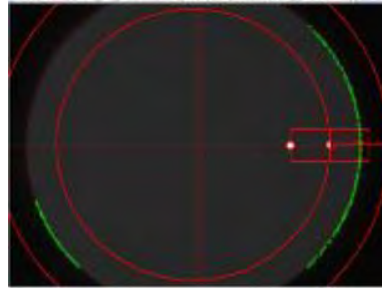


(Fig. 6a)

Optical metrology system



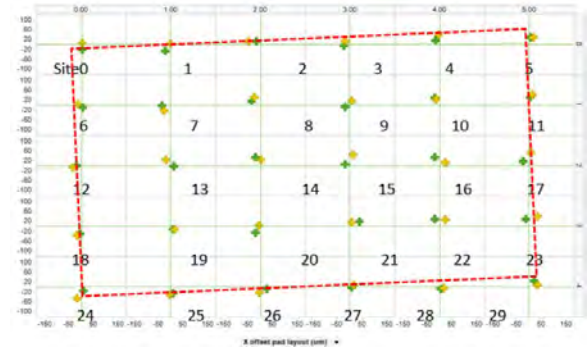
(Fig. 6b)



(Fig. 6c)

Each lens is measured detecting the contrast profile & transitions

Specific algorithms are automatically applied to locate the lens center

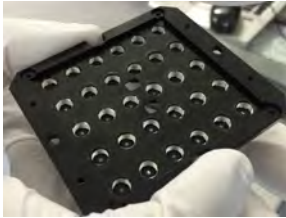


(Fig. 6d)

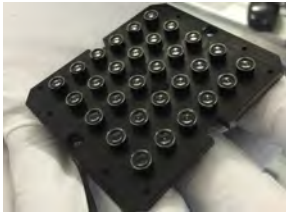
Validation

Lens Z tuning

- Tunable lens height in frame to reach +/- 25 um specification and ensure and site-to-site uniformity
 - Mechanical reference plane given by 1 reference tip
 - Tight fit assembly of the lens inside lens frame
- Lens driver to adjust the height by screwing, with known pitch threading



(Fig. 7a)



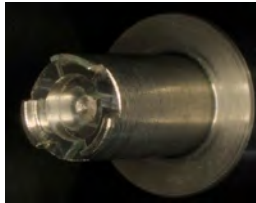
(Fig. 7b)

x30 lens frame



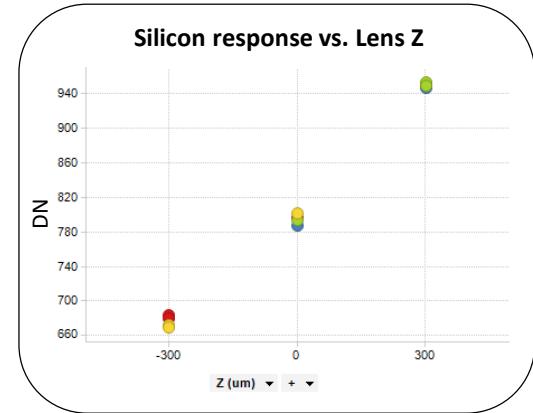
Lens (illumination side)

(Fig. 7c)



Lens driver head

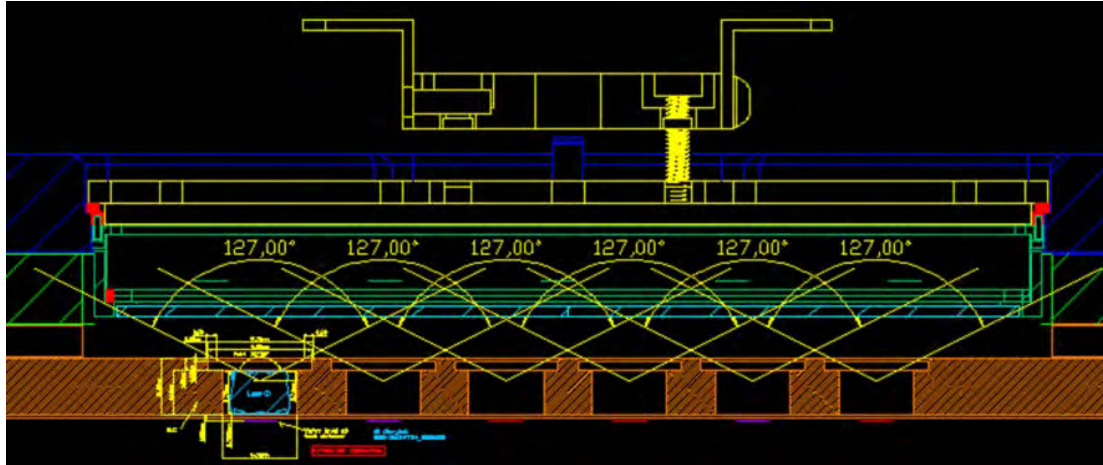
(Fig. 7d)



(Fig. 7e)

Site uniformity through 6x5 matrix

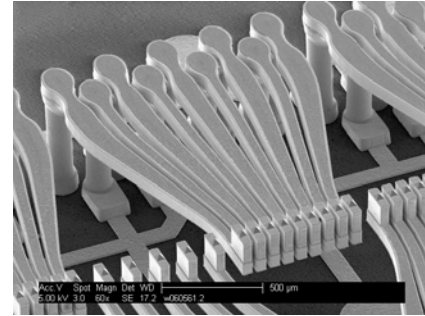
- Same quantity of incident light for each site has to be transferred through the diffuser
 - Enlarged diffuser is a key enabler for edge and corner sites on 6x5 matrix
 - Mechanical chamfer per site to use whole lens field of view



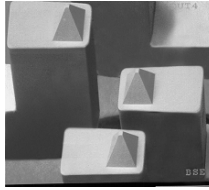
(Fig. 8)

Probes tips

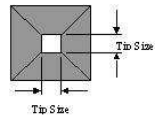
- T3+ FormFactor MicroSprings, 3D MEMS proprietary process
 - Spring geometry in all 3 dimensions, angled/curved probes for fan-out are possible (e.g. 6 x 5 DUT Layout)
 - Well adapted for high parallelism, especially for image sensor preventing any shadowing on image
- Design optimized for
 - Low Scrub Ratio (19%), 8.5 μm x 8.5 μm typical tip size
 - Fine Pitch (Min. 60 μm pitch)
 - Low probe force (1 g/mil)
 - Best contact performance



(Fig. 9a)



(Fig. 9b)



(Fig. 9c)

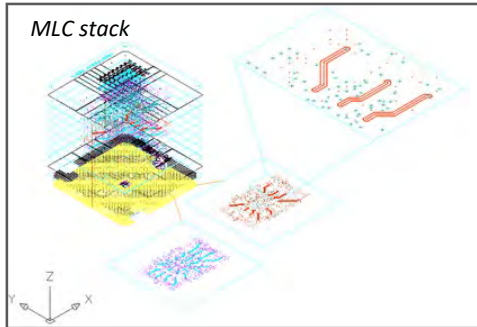
Signal integrity for high data rates

- High speed signal integrity along the whole signal path
 - -2.3 dB @1.5 Gbps data rate

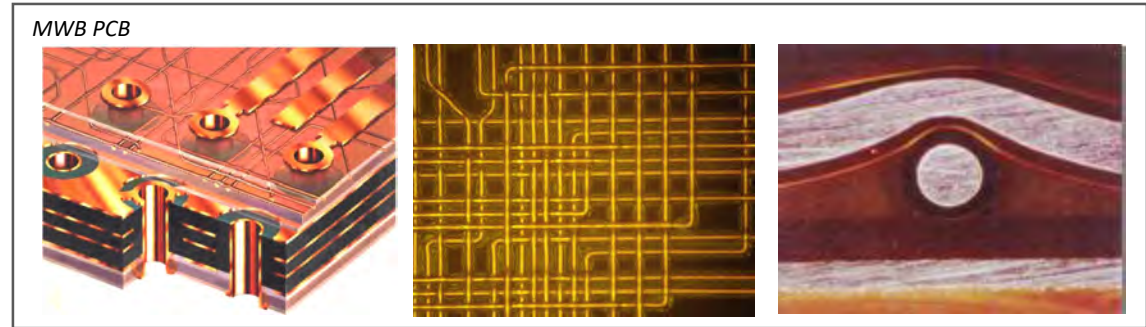
- Obtained by MLC combined with PCB hybrid technologies



(Fig. 10a)



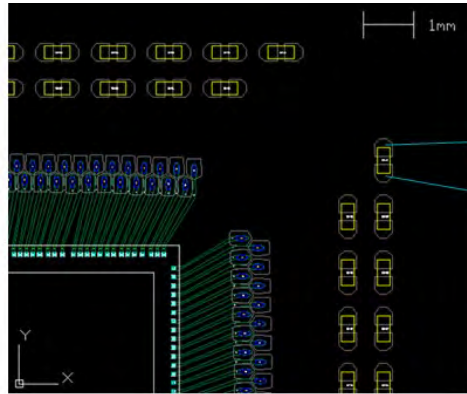
(Fig. 10b)



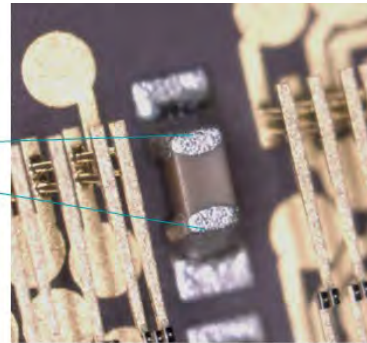
(Fig. 10c)

Power decoupling

- Very highly controlled power delivery is mandatory for each of 30 test sites
- For each of them power delivery impedance is simulated and implemented in the most ideal scenario i.e. decoupling capacitors are at the closest possible distance from the VDD pads of the die



(Fig. 11a)



(Fig. 11b)

Example of decoupling caps on MLC, wafer side

Conclusion

- Feedback from past experience
 - Capability to duplicate probe cards from Engineering to Mass Production
 - >1 million touch down without any incident linked to probe card
 - Very efficient probe alignment on pads
 - Stability in term of performances
 - Good probe card ageing
- Strong collaboration within the team between FFI & ST, key enabler to meet the specifications and to succeed
 - Regular F2F meetings & weekly calls
 - Multisite Japan/Italy/France
- Let's continue good collaboration on new products & challenges !

Thanks!

Q & A



Information and picture credits

Figure / Information

Credit

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Fig. 10c:	Takehisa Sakurai , Hiroyuki Yamaguchi, SWTW 2019 San Diego (CA), US.
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